A GaAs MMIC TRANSCEIVER FOR 2.45 GHz WIRELESS COMMERCIAL PRODUCTS

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ABSTRACT

Recent availability of unlicensed frequency bands (FCC part 15.247 and International Standards) has stimulated development of wireless products ranging from wireless LAN, PBX to data collection devices. This paper describes development and performance characteristics of an advanced MMIC transceiver that provides half duplex conversion between 2.4GHz and 915MHz. The chip is mounted in a 28-lead cofired ceramic package suitable for surface mount assembly. The highly integrated chip minimizes external components and can be readily implemented into miniature, low profile products such as the PCMCIA format.

INTRODUCTION

Commercial chips for wireless applications are under active development within the microwave industry. Prior component designs [1,2, and 3] have demonstrated relatively small subcircuit blocks such as power amplifiers, T/R switches, mixers, and LNA's. Continued system cost and size reduction has driven circuit design to higher levels of integration and increased circuit density. An example of more complex circuitry that provides transceiver or transverter functionality has been reported by GEC-Marconi[4]. Issues remain in partitioning technology choices (eg. Si vs GaAs), device processing (via holes, lithography) as well as wafer process yields.

The work reported here was driven by these (cost) considerations and performance requirements for a direct sequence spread spectrum modulation system operating at data rates exceeding 2Mbs. A critical design parameter is the minimization of spectral regrowth during data transmission in multi-channel applications. The chip can also function effectively in system architectures utilizing frequency hopping [5] or unspread modulation bandwidths. With constant envelope modulation formats, where saturated operation is allowed, higher power efficiency performance is obtained.

The design was targeted to operate at ±5 volt consistent with typical system requirements. The transmitter circuitry is capable of 5dB to 10dB greater power than previously reported transceiver chips at 2.45Ghz. Power and gain control of the transmitter is also provided. Throughout the chip, diode logic is used to provide control of functionality including power setting, receive gain steps and sleep mode settings.

The chip utilizes an intermediate frequency of 915MHz rather than 300MHz or 350MHz. The higher IF allows LO, harmonic, and inter-modulation products that can be suppressed by on-chip filtering and balancing. In contrast, a 300MHz IF requires a local oscillator frequency within 12% of the channel frequency. More external filtering is required. Another reason for this particular IF selection is the large product base in the 915MHz ISM band can be translated into 2.45GHz operation with this chip.

PROCESS DESCRIPTION

The MMIC was realized in a mature, 0.5 micron ion implanted MESFET process that includes via holes, TaN thin film resistors, GaAs mesa resistors, and MIM capacitors. Gates are written with E-beam lithography. This technology provides high yields in a 4" wafer process for both active and passive components. The chip area is approximately 22mm^2 and utilizes via holes to maximize chip functionality, circuit density, and provide critical isolation within the chip. Both the chip size and its process complexity have demonstrated yields necessary for viable commercial volumes and is considered a breakthrough for MMIC processing capability. Foundry loading achieved by the larger chip size allows a path to lower overall wafer costs , thereby producing competitive component costs. The MESFET process is based on a double recessed structure for power and T/R switch performance and contains both single and dual gate devices. The dual gate FETs are used in active mixer and switching devices.

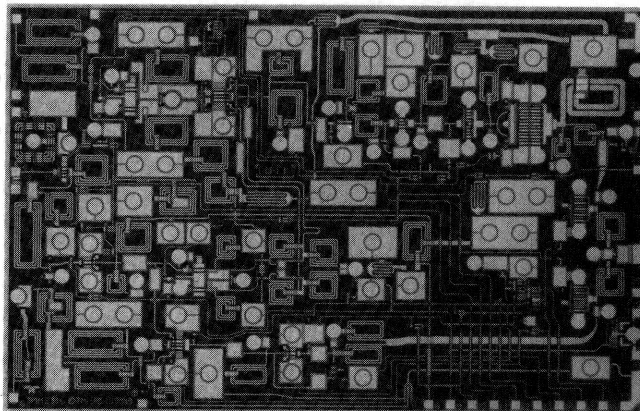

Fig. 1. 2.4GHz Transceiver Chip

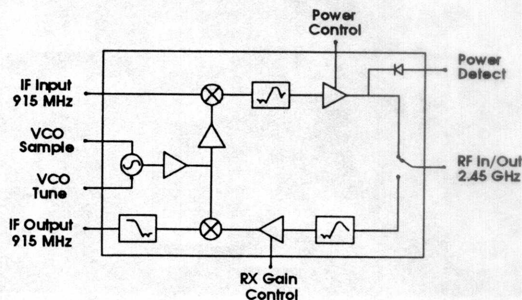

Fig. 2. 2.4GHz Transceiver Chip Block Diagram

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DESIGN

The chip architecture can be seen in the photomicrograph of Figure 1, and in the abbreviated block diagram of Figure 2. The LO is common to both transmit and receive paths and is tunable (VCO) from 1400MHz to 1650MHz. The VCO circuit is located near the center of the left edge of the chip. The LO function is fully integrated with the exception of a Silicon varactor tuning diode, placed within the package. (MMIC integrable varactor diodes are not yet available as standard foundry elements.) The oscillator is realized with a Colpitts topology. A single gate 250μm MESFET is used in this circuit. A posted (air-bridge suspended) rectangular inductor provides oscillator tank Q's above those of the other integrated tuning elements. A local oscillator sample port provides output for phase locked operation. VCO control voltage tuning range is 0.5V to 3.5V. With an external PLL , oscillator stability can be set to better than 75kHz.

Two stages of local oscillator (LO) buffering are provided in the up converter chain; however, the receive path down converter shares one of these stages. The second LO buffer provides balanced (0° ,180°) output to the transmitter mixer for upconversion. Second harmonic traps are provided at this interface. The first LO buffer active device is a 170μm dual gate MESFET. Single gate 250μm FETs are used in the second buffer/ϕ-splitter circuit as a differential pair circuit.

The transmitter signal path is comprised of seven stages. The 915MHz IF input signal is applied at the upper left corner of the chip. From left to right, the first stage is an IF buffer/ϕ-splitter circuit similar to the second LO buffer. Balanced IF buffer output is applied to the transmit mixer. A pair of 250μm dual gate FETs are operated in a balanced configuration where 1st gates are driven by balanced IF and 2nd gates are driven by balanced LO signals. Following the IF buffer and mixer are four stages of power amplification. The PA output stage is located in the upper right corner of the chip. A Schottky diode output power sensor circuit can also be seen there. Single gate MESFETs are used in all stages of the PA. The respective gate widths are 150μm, followed by 300μm, 600μm, and 3.0mm. Figure 3 photomicrograph of a three stage PA chip that is essentially the same as the last three stages of the transmitter. The three stage PA chip was developed previuosly and used as a basis for the transmitter chain. The characteristics of this amplifier have been previously described [6]. Second harmonic trap for high efficiency and spectral performance is included in the drain network of the final amplifier. Typical output power of 24dbm and transmit conversion gain of 30db are achieved including T/R switch losses. The transmit gain can be set in the range 20dB-35dB, by an analog control signal. Typical transmit mode currents are from 350-550mA depending on user-selected output power levels that can be adjusted from 20dBm to 24dBm.

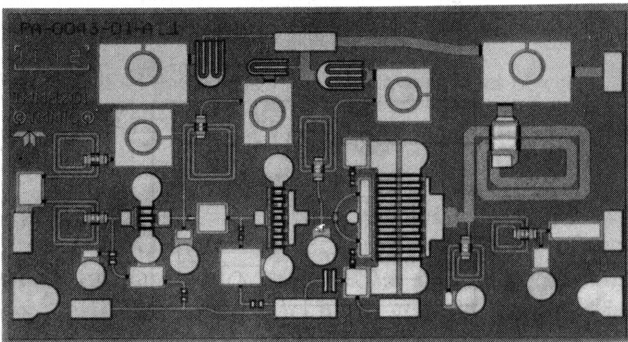

Fig. 3. 2.45GHz Power Amplifier Chip

The receiver is comprised of two active stages, an amplifier and a mixer. The receiver input amplifier uses a 125μm dual gate MESFET. A MESFET switch in a negative feedback path provide a controlled 26 dB gain step. Following the frontend amplifier is an unbalanced FET mixer. A 300μm dual gate MESFET is used here. As in the transmit mixer, LO is injected into the 2nd gate. An IF lowpass filter follows the receive mixer. Receiver output at 915MHz is available at the lower left corner of the chip. In receive mode , the chip can be set to a high and low gain state separated by 26db. Gain in the high state is from 5dB to 6dB and includes losses from on-chip input filtering as well as T/R switch. Typical receive mode currents around 90ma are achieved, including the LO and other support circuitry.

The T/R switch is located near the center of the right side. The switch circuit is a shunt form where 1.25mm dual gate MESFETs are connected to the ends of lumped equivalent ¼ λ transmission lines.

Ample on chip decoupling and bypassing is provided in the integrated bias distribution networks.

SPECTRAL PERFORMANCE

Spurious output performance of this chip is excellent. Figure 4 illustrates the unfiltered output from a typical unit in direct sequence spread spectrum transmit mode. It should be noted that the dominant output "*line*" corresponds to a single tone power of +20dBm. From Figure 4, the seven most significant output components are as follows: Lower sideband (654MHz), LO (1.569GHz), 2xIF (1.83GHz), 2xLO-IF (2.223GHz), RF (2.48GHz), 3xIF(2.75GHz), and 2xLO (3.138GHz). This spurious response satisfies the MKK requirements (Japan). Performance is essentially the same shifted 42MHz for US operation.

On chip filtering, beyond the interstage bandpass tuning, is as follows: Lowpass IF filter in receiver. Second harmonic traps in LO chain. Lower sideband suppression and LO second harmonic rejection is encorporated in the first PA stage. RF output second harmonic rejection is also provided in the final amplifier. The double balanced FET mixer provides additional rejection of the LO, IF, 3xIF, and 2xLO-IF spurs.

It is noteworthy that the highest amplitude spur is at 2xLO. A 915MHz IF places this spur away from the desired channel by **twice** the percent bandwidth offset as with a 300MHz IF.

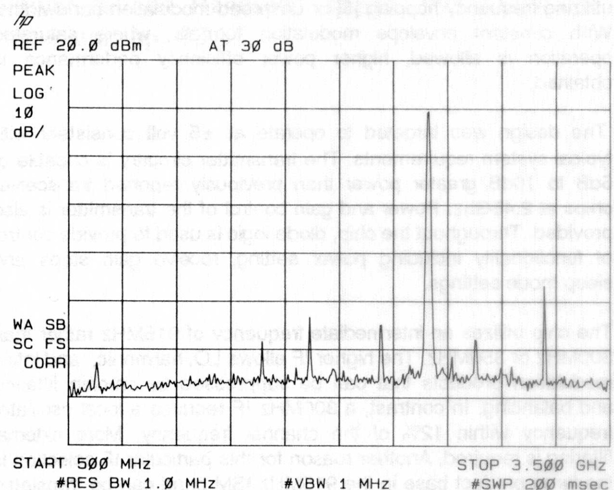

Fig. 4. Spectral Output of Transmitter

PACKAGING

A critical element to the transceiver performance is packaging. The product required development of an SMT-compatible, 28-lead package that can support 2.5 GHz operation and provide low thermal resistance. Figure 5 shows an approach using a 28 lead cofired ceramic package that contains both Copper and Kovar in its base providing low thermal resistance to the MMIC while maintaining the long term reliability of both chip and package. This package has been demonstrated to provide low loss and good VSWR (<2:1) extending beyond 10 GHz. The figure also shows two external multi-section capacitors that are realized on a high dielectric (ε_r=8000) substrate to provide signal isolation and DC supply line decoupling. The remaining bias networks are realized on-chip to minimize overall component count. Figure 6 illustrates the packaged transceiver installed in a final product.

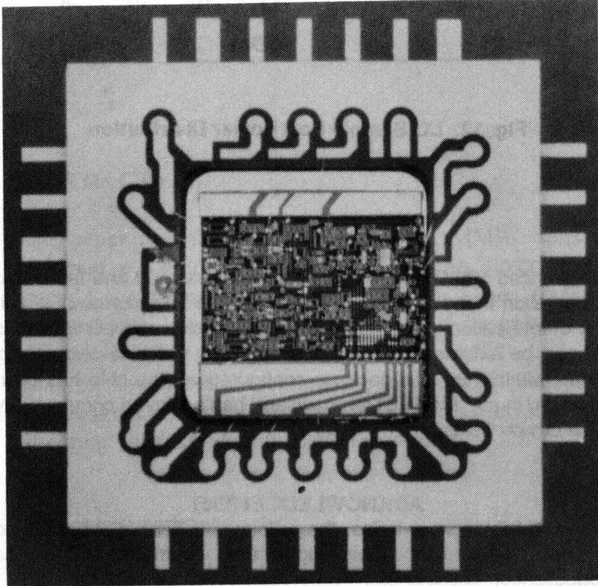

Fig. 5. Packaged Transceiver

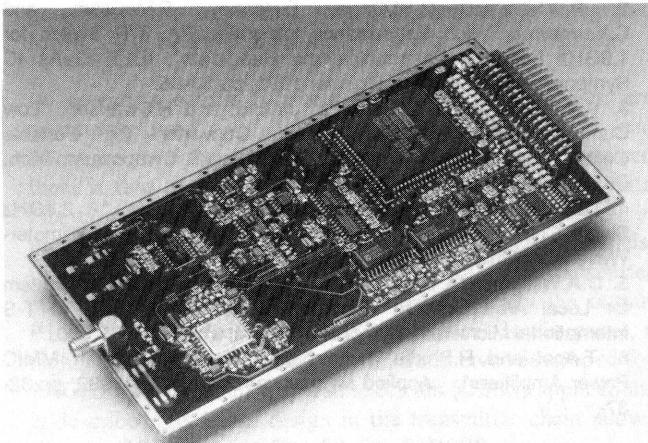

Fig. 6. Transceiver In SMT Environment

MEASURED PERFORMANCE

Measured performance of the transceiver's transmit path with a -4 dBm spread spectrum input signal at 915 MHz and output power of 20.5 dBm at 2.484 GHz is show in Figure 7. Sidelobe regeneration of a spread spectrum signal is typically -20 dBm under these test conditions. The spurious response of the transceiver is shown in Figure 4 again measured with spread spectrum input signal and 2.45 GHz output power of 20.5 dBm. The significant 3rd order intermodulation product of 2xLO-IF is typically -31.0 dBm under these test conditions while the 2nd harmonics of IF and LO are typically -26.0 and -32.0 dBm respectively.

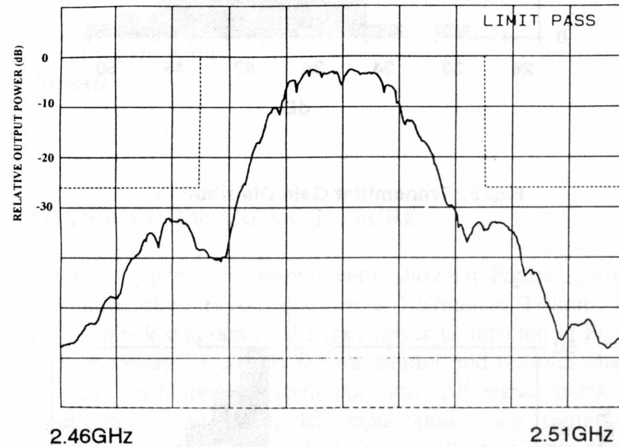

Fig. 7. Sidelobe Regrowth of SS Signal

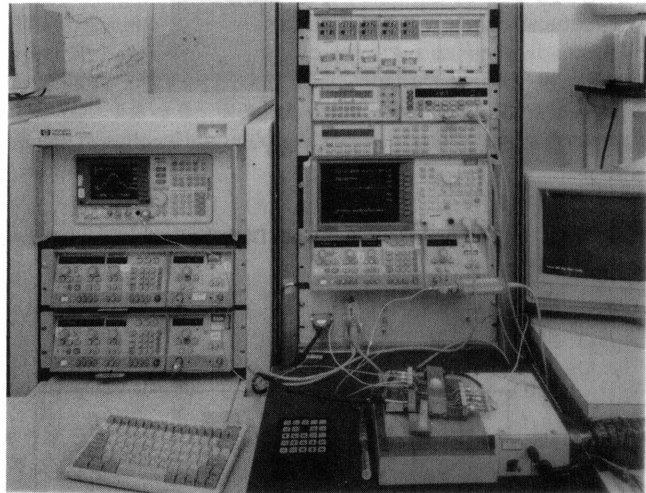

Fig. 8. Automated Test System

An automated electrical test system has been designed to measure critical performance parameters and track performance throughout production. This can be seen in Figure 8. Devices from more than 30 wafers spanning several lots of both 3" and 4" wafers have been characterized with extremely uniform results. Figure 9 shows a histogram of minimum transmit path small signal gain over a sample of 79 parts. Figures 10 and 11 show histograms of minimum receive path gain and receive path gain step over a sample of 229 parts. As a measure of the performance and

repeatability of the on-board LO, Figure 12 shows a histogram of the power available at the VCO Sample port for 229 parts.

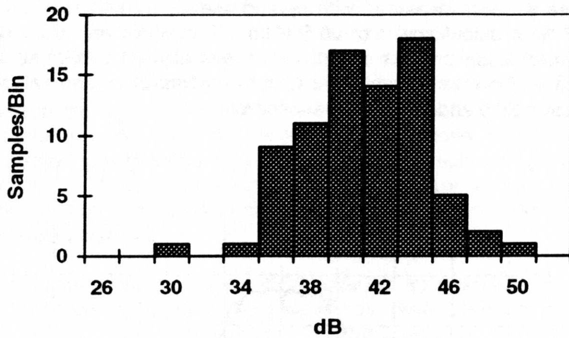

Fig. 9. Transmitter Gain Distribution

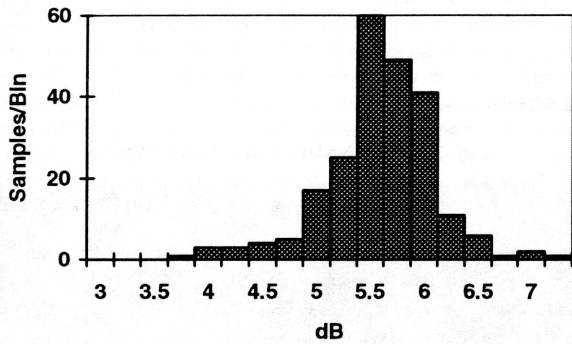

Fig. 10. Receiver Gain Distribution

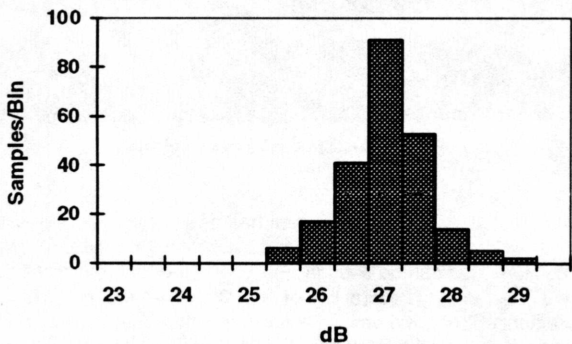

Fig. 11. Receiver Gain Step Distribution

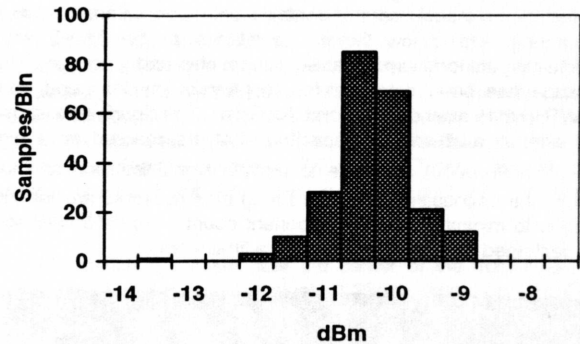

Fig. 12. LO Sample Port Power Distribution

CONCLUSIONS

An advanced MMIC transceiver has been designed and fabricated for operation in the 2.45GHZ ISM band. The chip contains a high level of integration including all transmit, receive and LO functions that can be externally controlled through ±5 volt bias and control signals within a 28 lead package configuration. The chip has been fabricated in a 4" MESFET process and has achieved commercially viable device yields.

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